SAURABH SUMAN

Jabalpur (M.P.), India | saurabhyahihai@gmail.com | linkedin/saurabhyahihai

SKILLS

C, C++, Python, Verilog, MATLAB, LTspice, KiCad; FPGA, Microcontrollers, Embedded Systems, IoT; SPI, I2C, UART, LoRa; Quantum Computing

EXPERIENCE

Indian Institute of Technology Kharagpur, India — *Research Intern*

MAY 2025 - AUG 2025

- Designed LoRa-FPGA communication systems for low-power IoT applications under the supervision of Prof. Sudip Misra

IoT & Robotics Lab, JEC Jabalpur — *Student Coordinator*

DEC 2024 - PRESENT

EDUCATION

Jabalpur Engineering College, India — *BTech (Electronics and Telecommunication Engineering)*

AUG 2023 - 2027

Relevant coursework: Embedded and Communication Systems, DSP, Semiconductors

PROJECTS

LoRa+FPGA Gateway System

- FPGA-based LoRa gateway using Tang Nano 20K and RFM96W module
- Implemented SPI protocol in SystemVerilog; simulated using ModelSim

MazeSolver Bot (eYRC 2025-26)

- Navigates using FPGA-implemented shortest-path algorithms, integrates sensing, and reports data via Bluetooth in a warehouse-like environment

TeleQ (Quantum Communication Demo)

- Demonstrated secure communication using quantum teleportation protocol

ACHIEVEMENTS

- Top-100 internationally — e-Yantra Robotics Competition (2025-26)
- Chief Minister's Meritorious Scholarship (full tuition)
- MIT iQuHACK 2025 participant